BATRON



# Specification for
# BTHQ 128064AVE-FETF-06-LEDWHITE-COG

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supplied Midas Components Ltd -- Tel : +44 1493 602602 -- www.midascomponents.co.uk

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# CONTENTS

**Specification**
**of**
**LCD Module Type**
**Model No.: COG-BTHQ12864-03**

## 1. General Description

- 128 x 64 dots FSTN Positive Black & White Transflective Dot Matrix LCD Module.
- Viewing Angle: 6 o'clock direction.
- Driving duty: 1/65 duty, 1/7 bias.
- 'Epson' SED1565D0B (COG) Dot Matrix LCD Driver.
- 8080 Series MPU interface (default).
- 6800 Series MPU interface (Optional).
- FPC.
- White LED05 backlight.

## 2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

| Parameter | Specifications | Unit |
|---|---|---|
| Outline dimensions | 89.7(W) x 49.8(H) x 6.0(D)(Exclude FPC & gate)<br>89.7(W) x 149.8(H) x 6.0(D)(Include FPC. Exclude gate)<br>89.7(W) x 150.0(H) x 6.0(D)(Include FPC and gate) | mm |
| View area | 66.8 MIN.(W) x 35.5 MIN. (H) | mm |
| Active area | 63.985(W) x 31.985(H) | mm |
| Display format | 128 (W) x 64(H) | dots |
| Dot size | 0.485(W) x 0.485(H) | mm |
| Dot spacing | 0.015(W) x 0.015(H) | mm |
| Dot pitch | 0.500(W) x 0.500(H) | mm |
| Weight: | TBD | grams |

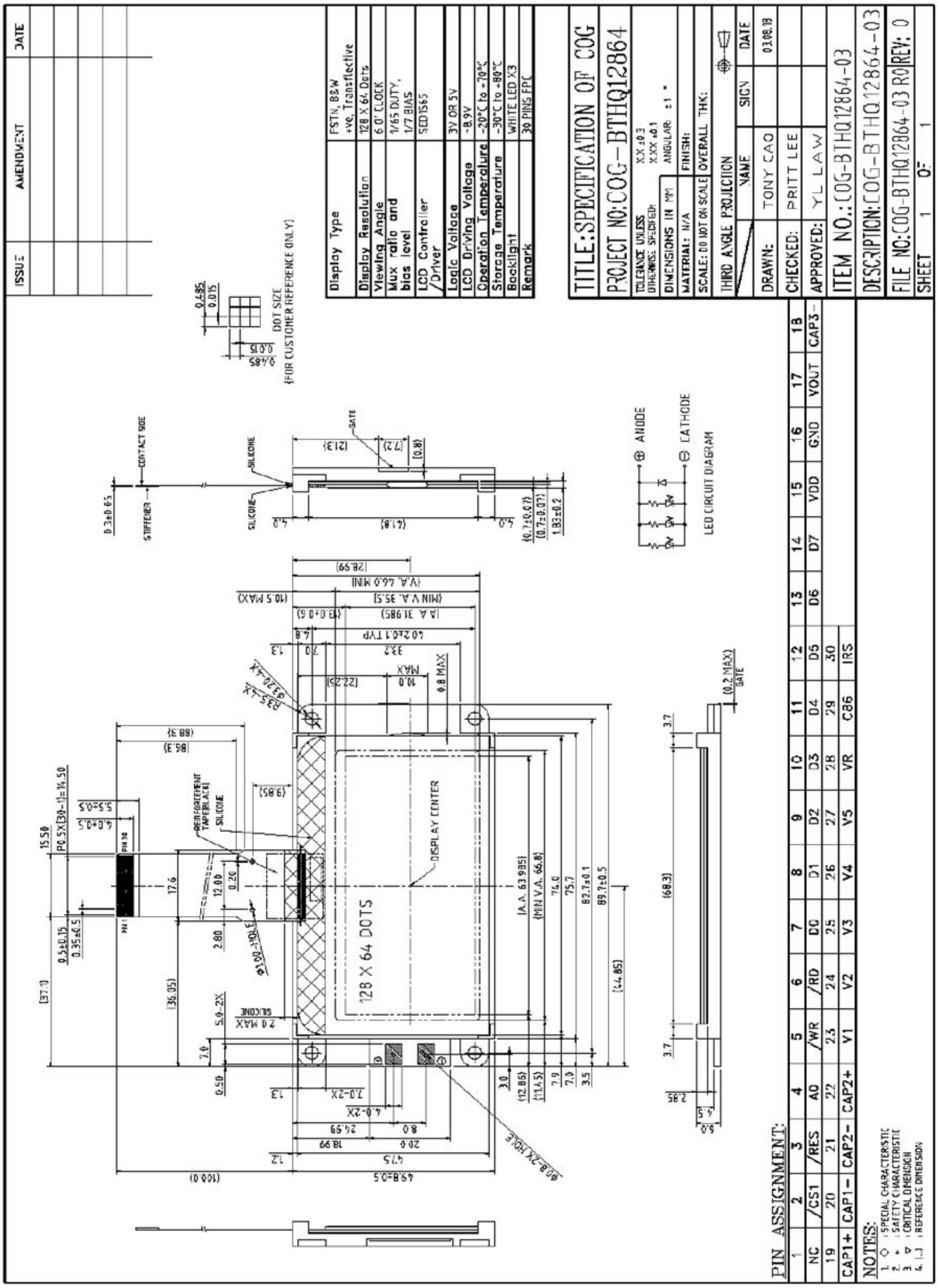



Figure 1: Module Specification

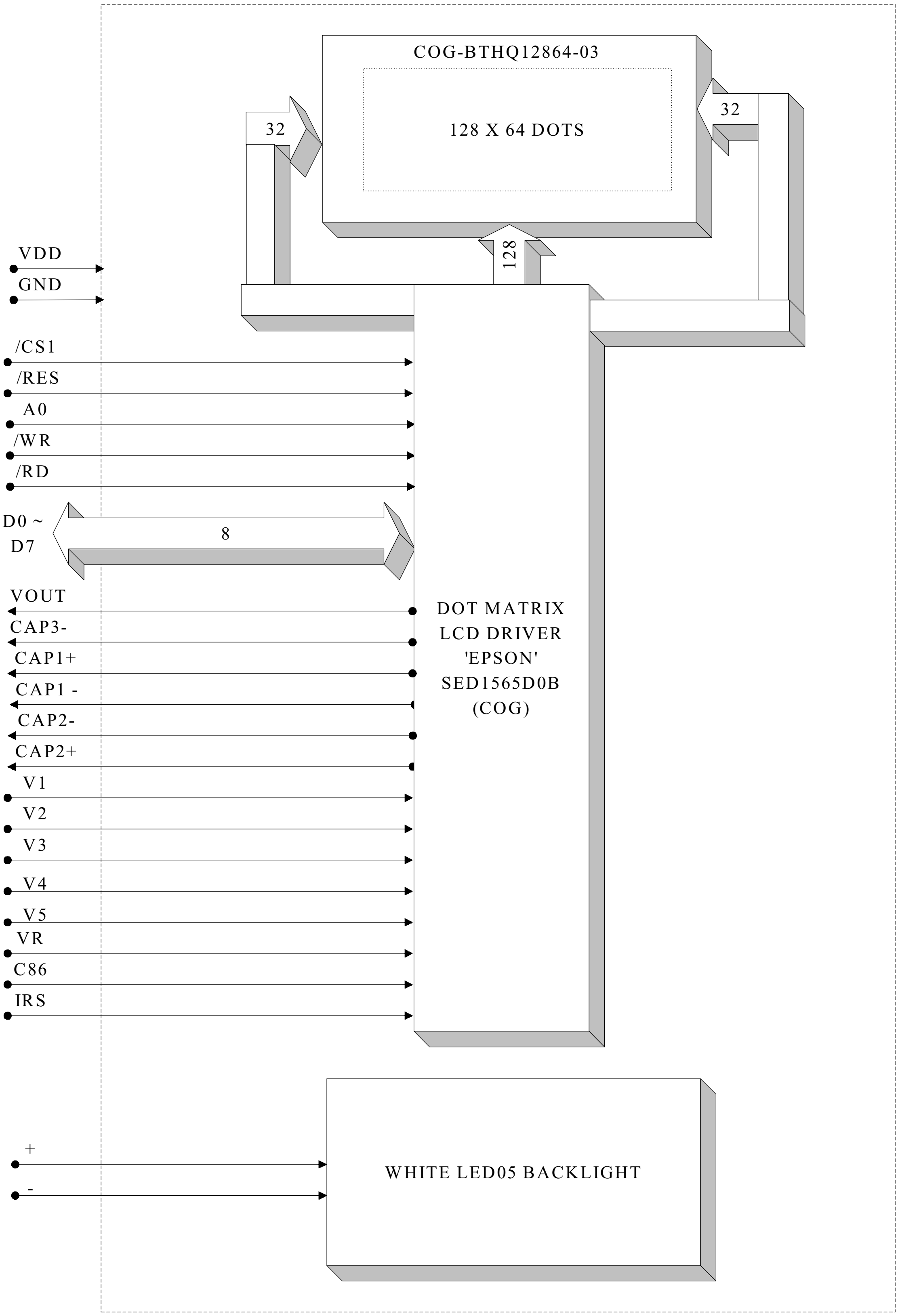



Figure 2: Block Diagram

## 3. Interface signals

Table 2 (a)

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | NC | No connection. |
| 2 | /CS1 | This is the chip select signal. When /CS1 = "L", then the chip select become active, and data/command I/O is enabled. |
| 3 | /RES | When /RES is set to "L," the settings are initialized. The reset operation is performed by the /RES signal level. |
| 4 | A0 | This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command.<br>A0 = "H": Indicates that D0 to D7 are display data.<br>A0 = "L": Indicates that D0 to D7 are control data. |
| 5 | /WR | When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. |
| 6 | /RD | When connected to an 8080 MPU, this is active LOW.<br>This pin is connected to the /RD signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L". |
| 7 | D0 | This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit 8 standard MPU data bus. |
| 8 | D1 | |
| 9 | D2 | |
| 10 | D3 | |
| 11 | D4 | |
| 12 | D5 | |
| 13 | D6 | |
| 14 | D7 | |
| 15 | VDD | Power supply. Shared with the MPU power supply terminal VCC. |
| 16 | GND | Connection with ground. |
| 17 | VOUT | DC/DC voltage converter. Connect a capacitor between this terminal and GND . |
| 18 | CAP3- | DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. |
| 19 | CAP1+ | DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal. |
| 20 | CAP1- | DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal. |
| 21 | CAP2- | DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal. |
| 22 | CAP2+ | DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal. |

Table 2 (b)

| Pin No. | Symbol | Description |
|---|---|---|
| 23~ 27 | V1,V2, V3,V4, V5 | This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below.<br>VDD (= V0) ≧V1≧V2≧V3 ≧V4≧V5<br>Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.<br>For 1/7 bias: V1=(1/7)xV5, V2=(2/7)xV5, V3=(5/7)xV5, V4=(6/7)xV5. |
| 28 | VR | Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider.<br>These are only enabled when the V5 voltage regulator internal resistors are not used (IRS = “L”).<br>These cannot be used when the V5 voltage regulator internal resistors are used (IRS = “H”). |
| 29 | C86 | This is the MPU interface switch terminal.<br>C86 = “H”: 6800 Series MPU interface.<br>C86 = “L”: 8080 MPU interface. |
| 30 | IRS | This terminal selects the resistors for the V5 voltage level adjustment.<br>IRS = “H”: Use the internal resistors<br>IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.<br>This pin is enabled only when the master operation mode is selected.<br>It is fixed to either “H” or “L” when the slave operation mode is selected. |
| | + | Anode of backlight |
| | - | Cathode of backlight. |

## 4. Absolute Maximum Ratings

### 4.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 3

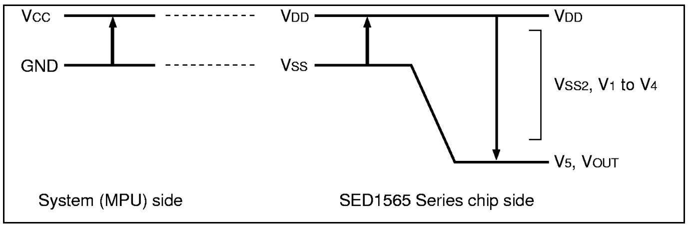
| Parameter | | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply voltage (Logic) | | VDD-GND =VDD-VSS | -0.3 | +7.0 | V |
| Power supply voltage (VDD standard) | | GND(=VSS2) | -7.0 | +0.3 | V |
| | With Triple set-up | | -6.0 | +0.3 | V |
| | With Quad step-up | | -4.5 | +0.3 | V |
| Power Supply voltage(V5,VOUT) (VDD standard) | | V5,VOUT | -18.0 | +0.3 | V |
| Power Supply voltage(V1~V4) (VDD standard) | | V1,V2,V3,V4 | V5 | +0.3 | V |
| Input voltage | | Vin | -0.3 | VDD+0.3 | V |

Note: 1.)The modules may be destroyed if they are used beyond the absolute maximum ratings.

2.) Insure that the voltage levels of V1, V2, V3, and V4 are always such that

$VDD \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$.

3.) The VSS2,V1 to V5 and VOUT are relative to VDD=0V reference.




### 4.2 Environmental Condition

Table 4

| Item | Operating Temperature (Topr) Min. | Operating Temperature (Topr) Max. | Storage Temperature (Tstg) Min. | Storage Temperature (Tstg) Max. | Remark |
|---|---|---|---|---|---|
| Ambient Temperature | -20°C | +70°C | -30°C | +80°C | Dry |
| Humidity | 95% max. RH for Ta ≤ 40°C<br>< 95% RH for Ta > 40°C | | | | no condensation |
| Vibration (IEC 68-2-6) cells must be mounted on a suitable connector | Frequency: 10 ~ 55 Hz<br>Amplitude: 0.75 mm<br>Duration: 20 cycles in each direction. | | | | 3 directions |
| Shock (IEC 68-2-27) Half-sine pulse shape | Pulse duration: 11 ms<br>Peak acceleration: 981 $m/s^2$ = 100g<br>Number of shocks: 3 shocks in 3 mutually perpendicular axes. | | | | 3 directions |

# 5. Electrical Specifications

## 5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, GND =0V.

Table 5

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (Logic) | VDD-GND | | 4.75 | 5.0 | 5.25 | V |
| Supply voltage (LCD) | VLCD =VDD-V5 | VDD = +5.0V, Note (1) | 8.6 | 8.9 | 9.2 | V |
| Low-level input signal voltage | $V_{ILC}$ | | GND | - | 0.2xVDD | V |
| High-level input signal voltage | $V_{IHC}$ | | 0.8xVDD | - | VDD | V |
| Supply Current (Logic & LCD) | IDD | VDD = 5V, Character mode | - | 0.5 | 0.7 | mA |
| | | VDD = 5V, Checker board mode | - | 1.1 | 1.3 | mA |
| Supply voltage of white LED05 backlight | VLED05 | Forward current =45mA<br><br>Number of LED dies =1x3=3 | 4.8 | 5.0 | 5.2 | V |

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

## 5.2 Timing Specifications

**Reset Timing**

**At Ta = -20 °C to +70 °C, VDD = +5.0V±5%, GND = 0V.**

Table 6

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Reset time | | $t_R$ | | — | — | 0.5 | µs |
| Reset "L" pulse width | RES | $t_{RW}$ | | 0.5 | — | — | µs |

Note: All timing is specified with 20% and 80% of VDD as the standard.

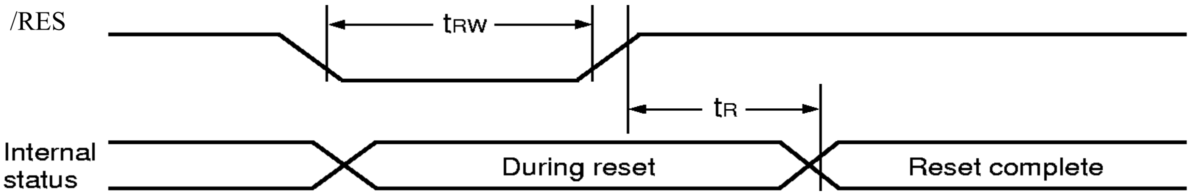



Figure 3:Reset Timing

**System Bus Read/Write Characteristics (8080 Series MPU)**

**At Ta = -20 °C to +70 °C, VDD = +5.0V±5%, GND = 0V.**

Table 7

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Address hold time | A0 | $t_{AH8}$ | | 0 | — | ns |
| Address setup time | | $t_{AW8}$ | | 0 | — | ns |
| System cycle time | A0 | $t_{CYC8}$ | | 166 | — | ns |
| Control L pulse width ($\overline{WR}$) | $\overline{WR}$ | $t_{CCLW}$ | | 30 | — | ns |
| Control L pulse width ($\overline{RD}$) | $\overline{RD}$ | $t_{CCLR}$ | | 70 | — | ns |
| Control H pulse width ($\overline{WR}$) | $\overline{WR}$ | $t_{CCHW}$ | | 30 | — | ns |
| Control H pulse width ($\overline{RD}$) | $\overline{RD}$ | $t_{CCHR}$ | | 30 | — | ns |
| Data setup time | D0 to D7 | $t_{DS8}$ | | 30 | — | ns |
| Address hold time | | $t_{DH8}$ | | 10 | — | ns |
| $\overline{RD}$ access time | | $t_{ACC8}$ | $C_L$ = 100 pF | — | 70 | ns |
| Output disable time | | $t_{OH8}$ | | 5 | 50 | ns |

*1 The input signal rise time and fall time ($t_r$, $t_f$) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \le (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \le (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.
*2 All timing is specified using 20% and 80% of $V_{DD}$ as the reference.
*3 $t_{CCLW}$ and $t_{CCLR}$ are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

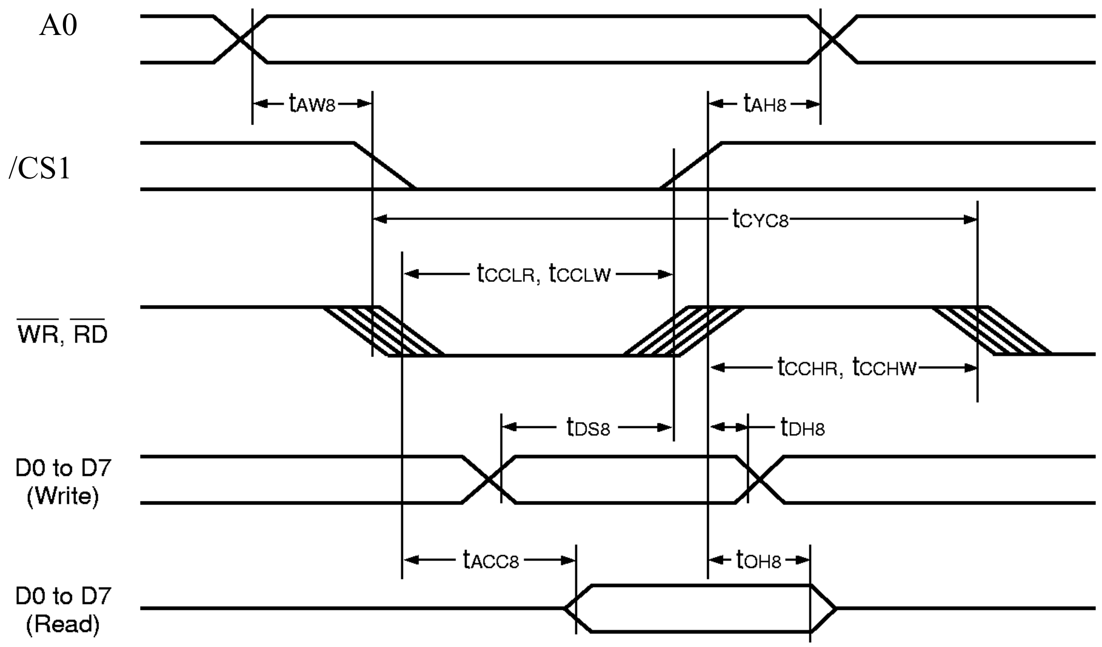



Figure 4: MPU bus read / write timing diagram (80 family MPU)

**System Bus Read/Write Characteristics (6800 Series MPU)**

**At Ta = -20 °C to +70 °C, VDD = +5.0V±5%, VSS = 0V.**

Table 8

| Item | | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min | Max | |
| Address hold time<br>Address setup time | | A0 | $t_{AH6}$<br>$t_{AW6}$ | | 0<br>0 | —<br>— | ns<br>ns |
| System cycle time | | A0 | $t_{CYC6}$ | | 166 | — | ns |
| Data setup time<br>Data hold time | | D0 to D7 | $t_{DS6}$<br>$t_{DH6}$ | | 30<br>10 | —<br>— | ns<br>ns |
| Access time<br>Output disable time | | | $t_{ACC6}$<br>$t_{OH6}$ | $C_L$ = 100 pF | —<br>10 | 70<br>50 | ns<br>ns |
| Enable H pulse time | Read<br>Write | E | $t_{EWHR}$<br>$t_{EWHW}$ | | 70<br>30 | —<br>— | ns<br>ns |
| Enable L pulse time | Read<br>Write | E | $t_{EWLR}$<br>$t_{EWLW}$ | | 30<br>30 | —<br>— | ns<br>ns |

*1 The input signal rise time and fall time ($t_r$, $t_f$) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \le (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \le (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.
*2 All timing is specified using 20% and 80% of $V_{DD}$ as the reference.
*3 $t_{EWLW}$ and $t_{EWLR}$ are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

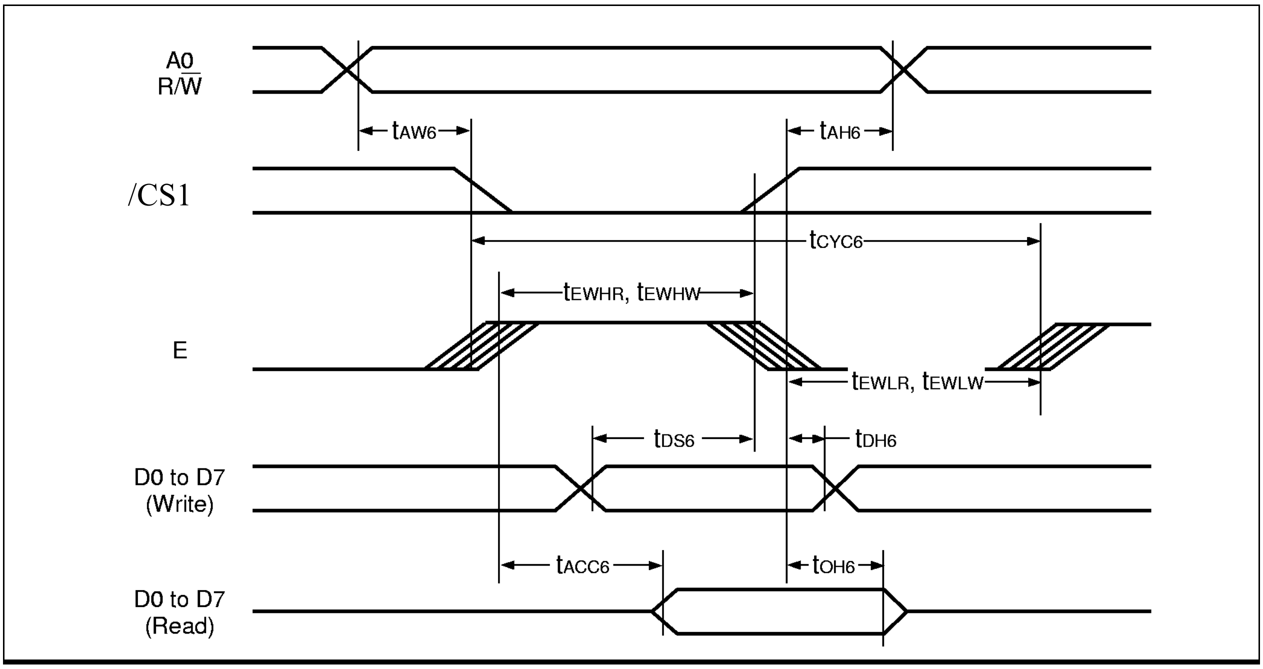



Figure 5: MPU bus read / write timing diagram (68 family MPU)

## 5.3 Instruction Set

Table 8

| | Command | Command Code | | | | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A0 | $\overline{RD}$ | $\overline{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (1) | Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0<br>1 | LCD display ON/OFF<br>0: OFF, 1: ON |
| (2) | Display start line set | 0 | 1 | 0 | 0 | 1 | Display start address | | | | | | Sets the display RAM display start line address |
| (3) | Page address set | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page address | | | | Sets the display RAM page address |
| (4) | Column address set upper bit | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Most significant column address | | | | Sets the most significant 4 bits of the display RAM column address. |
| | Column address set lower bit | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Least significant column address | | | | Sets the least significant 4 bits of the display RAM column address. |
| (5) | Status read | 0 | 0 | 1 | Status | | | | 0 | 0 | 0 | 0 | Reads the status data |
| (6) | Display data write | 1 | 1 | 0 | Write data | | | | | | | | Writes to the display RAM |
| (7) | Display data read | 1 | 0 | 1 | Read data | | | | | | | | Reads from the display RAM |
| (8) | ADC select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0<br>1 | Sets the display RAM address SEG output correspondence<br>0: normal, 1: reverse |
| (9) | Display normal/ reverse | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0<br>1 | Sets the LCD display normal/ reverse<br>0: normal, 1: reverse |
| (10) | Display all points ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0<br>1 | Display all points<br>0: normal display<br>1: all points ON |
| (11) | LCD bias set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0<br>1 | Sets the LCD drive voltage bias ratio<br>SED1565*** ....... 0: 1/9, 1: 1/7<br>SED1566***<br>/SED1568***<br>/SED1569*** ...... 0: 1/8, 1: 1/6<br>SED1567*** ....... 0: 1/6, 1: 1/5 |
| (12) | Read/modify/write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Column address increment<br>At write: +1<br>At read: 0 |
| (13) | End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Clear read/modify/write |
| (14) | Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Internal reset |
| (15) | Common output mode select | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0<br>1 | * | * | * | Select COM output scan direction<br>0: normal direction,<br>1: reverse direction |
| (16) | Power control set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Operating mode | | | Select internal power supply operating mode |
| (17) | V5 voltage regulator internal resistor ratio set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Resistor ratio | | | Select internal resistor ratio (Rb/Ra) mode |
| (18) | Electronic volume mode set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| | Electronic volume register set | 0 | 1 | 0 | * | * | Electronic volume value | | | | | | Set the V5 output voltage electronic volume register |
| (19) | Static indicator ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0<br>1 | 0: OFF, 1: ON |
| | Static indicator register set | 0 | 1 | 0 | * | * | * | * | * | * | Mode | | Set the flashing mode |
| (20) | Power saver | | | | | | | | | | | | Display OFF and display all points ON compound command |
| (21) | NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Command for non-operation |
| (22) | Test | 0 | 1 | 0 | 1 | 1 | 1 | 1 | * | * | * | * | Command for IC test. Do not use this command |

(Note) *: disabled data

## 6. Reference Application Circuit (8080) Example

